

TSMC-03-265



April 2, 2004

To: Commissioner for Patents  
P.O.Box 1450  
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572  
28 Davis Avenue  
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/757,203 01/14/04 |

Kuo-Chi Tu

A NOVEL RANDOM ACCESS MEMORY (RAM)  
CAPACITOR IN SHALLOW TRENCH ISOLATION  
WITH IMPROVED ELECTRICAL ISOLATION  
TO OVERLYING GATE ELECTRODES

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56.

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
deposited with the United States Postal Service as first class  
mail in an envelope addressed to: Commissioner for Patents,  
P.O. Box 1450, Alexandria, VA 22313-1450, on April 12, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 4/12/04

The 1T-SRAM is described in detail in "The Ideal SoC Memory: 1T-SRAM," Leung et al., pp. 32-36 in Proceedings of the IEEE 2000.

U.S. Patent 6,256,248 to Leung, "Method and Apparatus for Increasing the Time Available for Internal Refresh for 1-T SRAM Compatible Devices," discloses a memory system including a DRAM array, a read buffer, a write buffer and an input/output (I/O) interface.

U.S. Patent 6,468,855 to Leung et al., "Reduced Topography DRAM Cell Fabricated Using a Modified Logic Process and Method for Operating Same," discloses a memory system that includes a DRAM cell that includes an access transistor and a storage capacitor.

U.S. Patent 4,713,678 to Womack et al., "dRAM Cell and Method," describes a method for making a deep trench capacitor.

U.S. Patent 6,420,226 to Chen et al., "Method of Defining a Buried Stack Capacitor Structure for a One Transistor RAM Cell," describes a method for making a buried stacked capacitor structure in a shallow trench.

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U.S. Patent 6,580,110 to Schrems, "Trench Capacitor and Method for Fabricating a Trench Capacitor," describes making deep trench capacitors in a silicon substrate.

Sincerely,

A handwritten signature in black ink, appearing to read 'SBA', with a long horizontal flourish extending to the right.

Stephen B. Ackerman,  
Reg. No. 37761

Lynchpin Member

10/757,203

Kao-Chi Tu

01/14/04

Group 21 Unit

(Use several sheets if necessary)

APR 15 2004  
PATENT & TRADEMARK OFFICE

FOREIGN PATENT DOCUMENTS												
	DOCUMENT NUMBER						DATE	COUNTRY	CLASS	SUBCLASS	Translation	
											YES	NO

-	"The Ideal SoC Memory: 1T-SRAM", Leung et al., pp.32-36, Proceedings of the IEEE 2000.

DATE COMPLETED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.